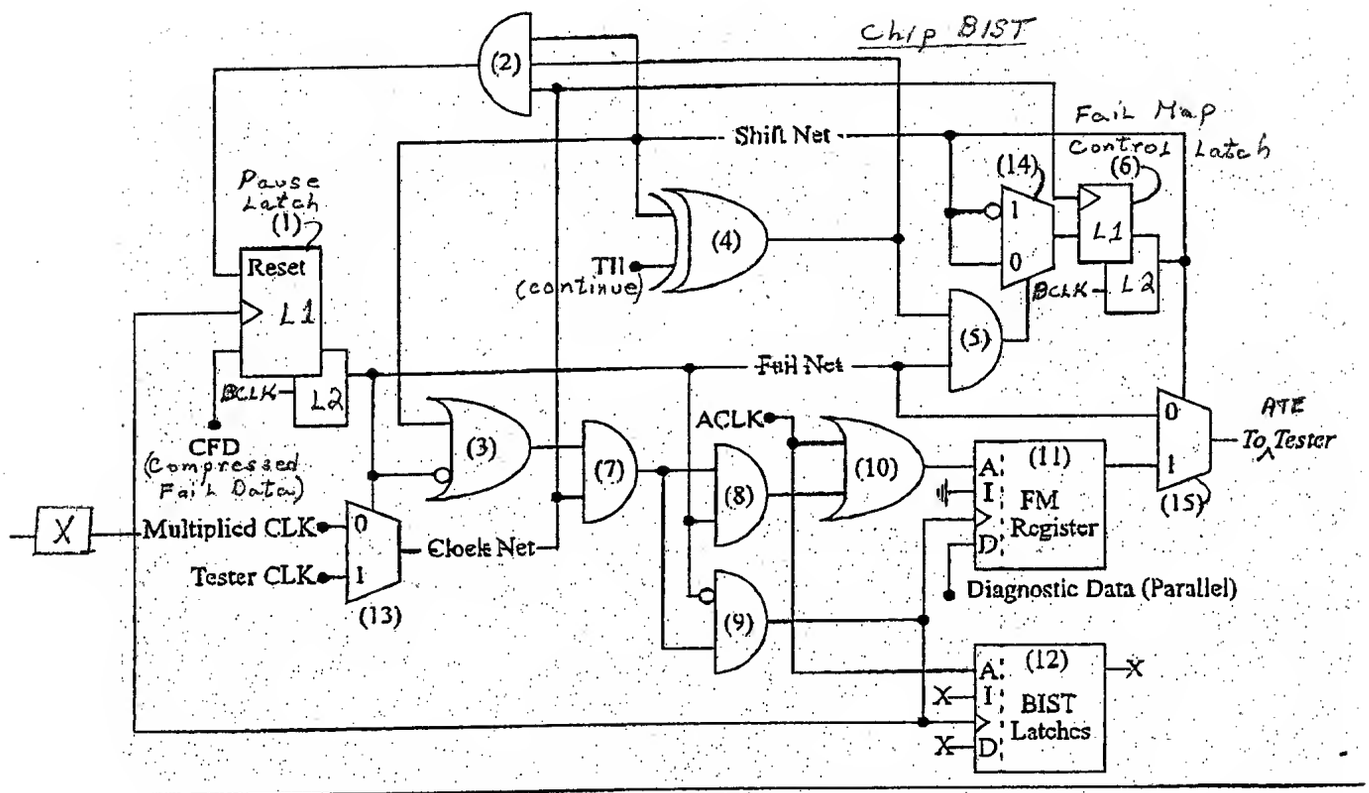

Figure 1: Fail Map Circuit

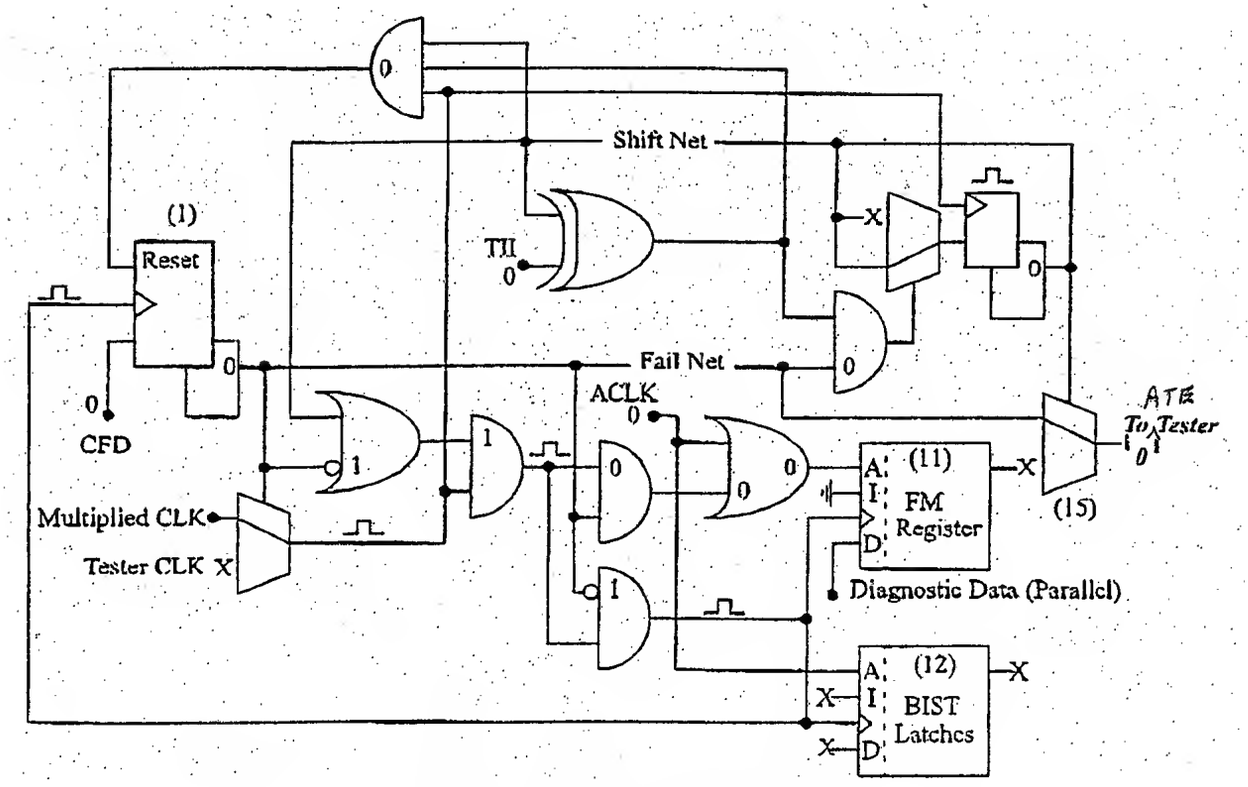

Figure 2: Fail Mapping before fail

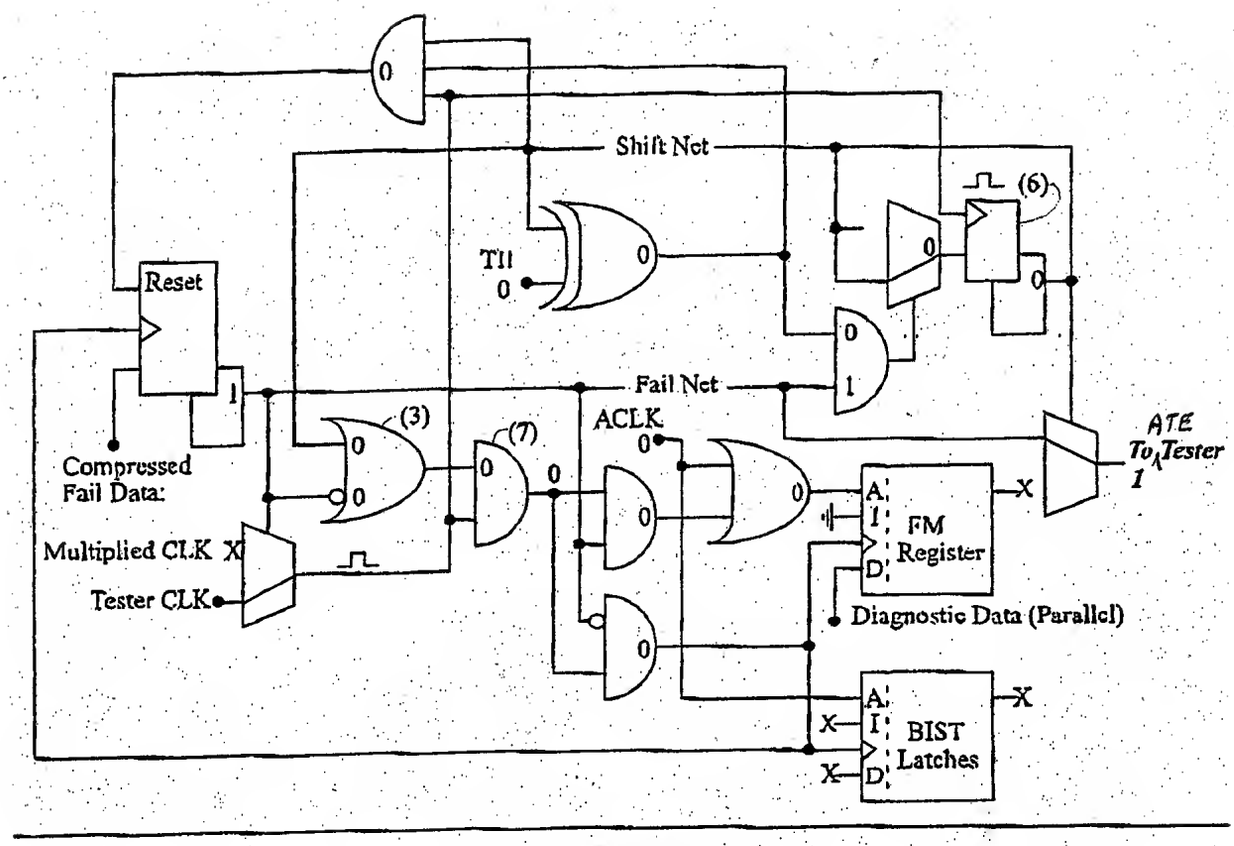

Figure 3: Fail Net asserted

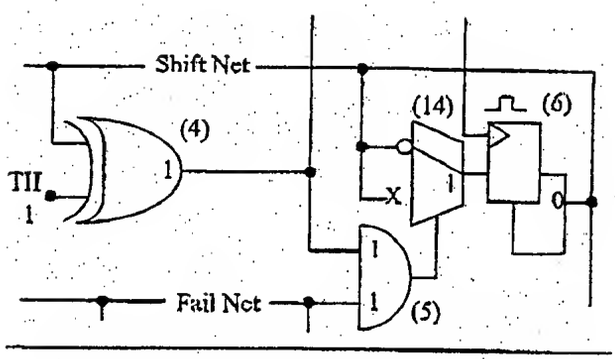

Figure 4: Asserting TII asserts Shift Net(+)

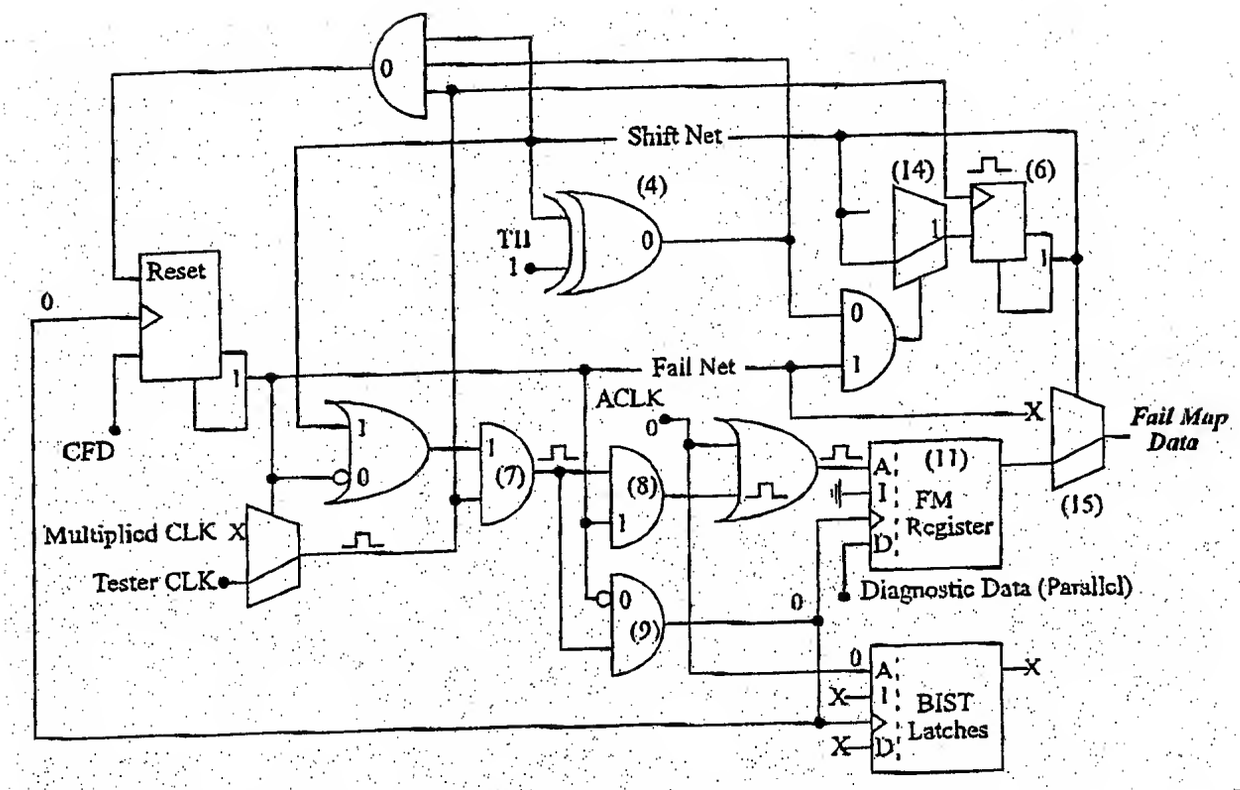

Figure 5: Fail Map Shift Out

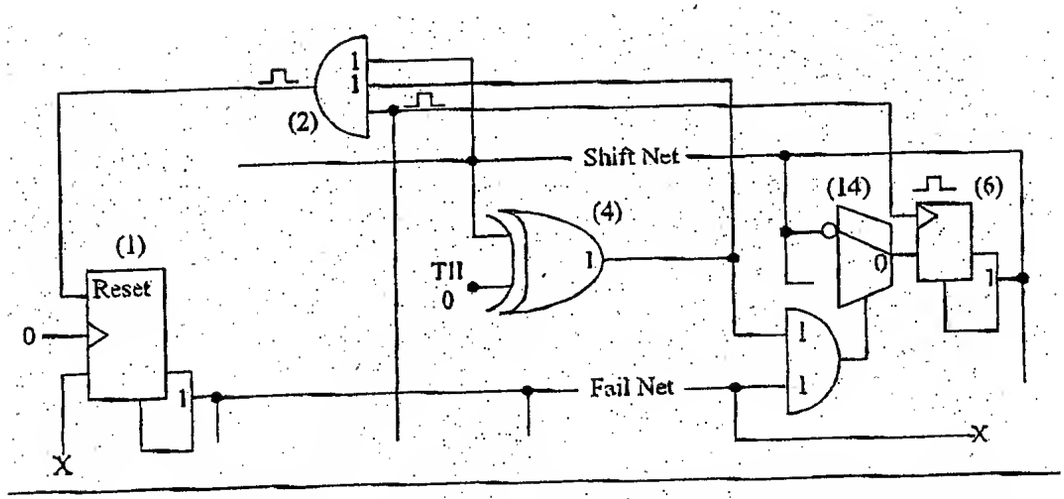

Figure 6: Clearing TII resets Latch 1 (Fail Net) and Latch 6 (Shift Net)

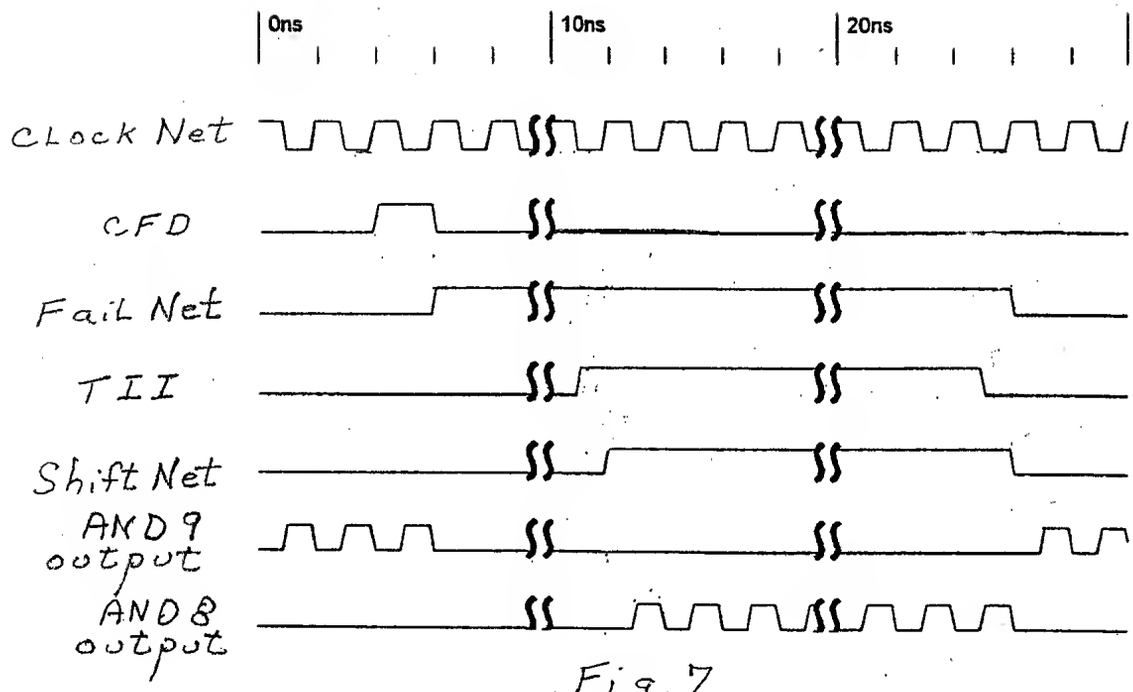
0ns
10ns
20ns
Clock Net
CFD
Fail Net
TII
Shift Net
AND 9 output
AND 8 output

Fig. 7

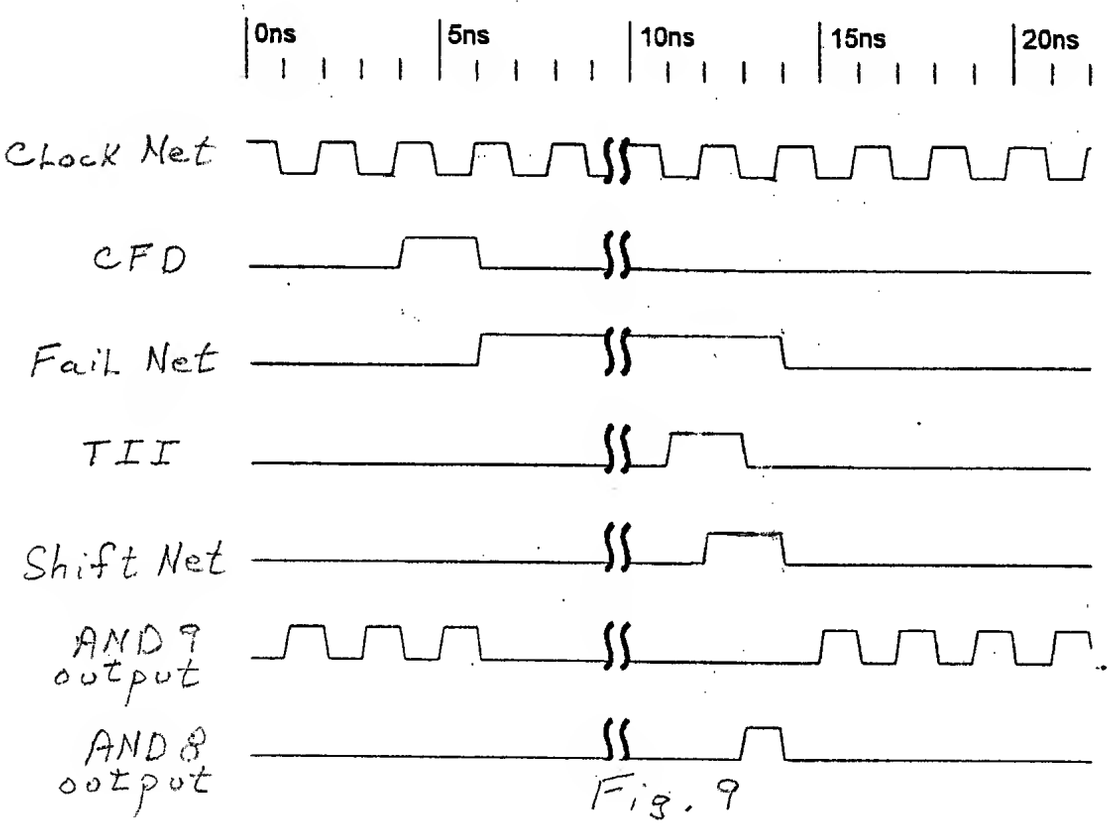
0ns
5ns
10ns
15ns
20ns
Clock Net
CFD
Fail Net
TII
Shift Net
AND 9 output
AND 8 output

Fig. 9

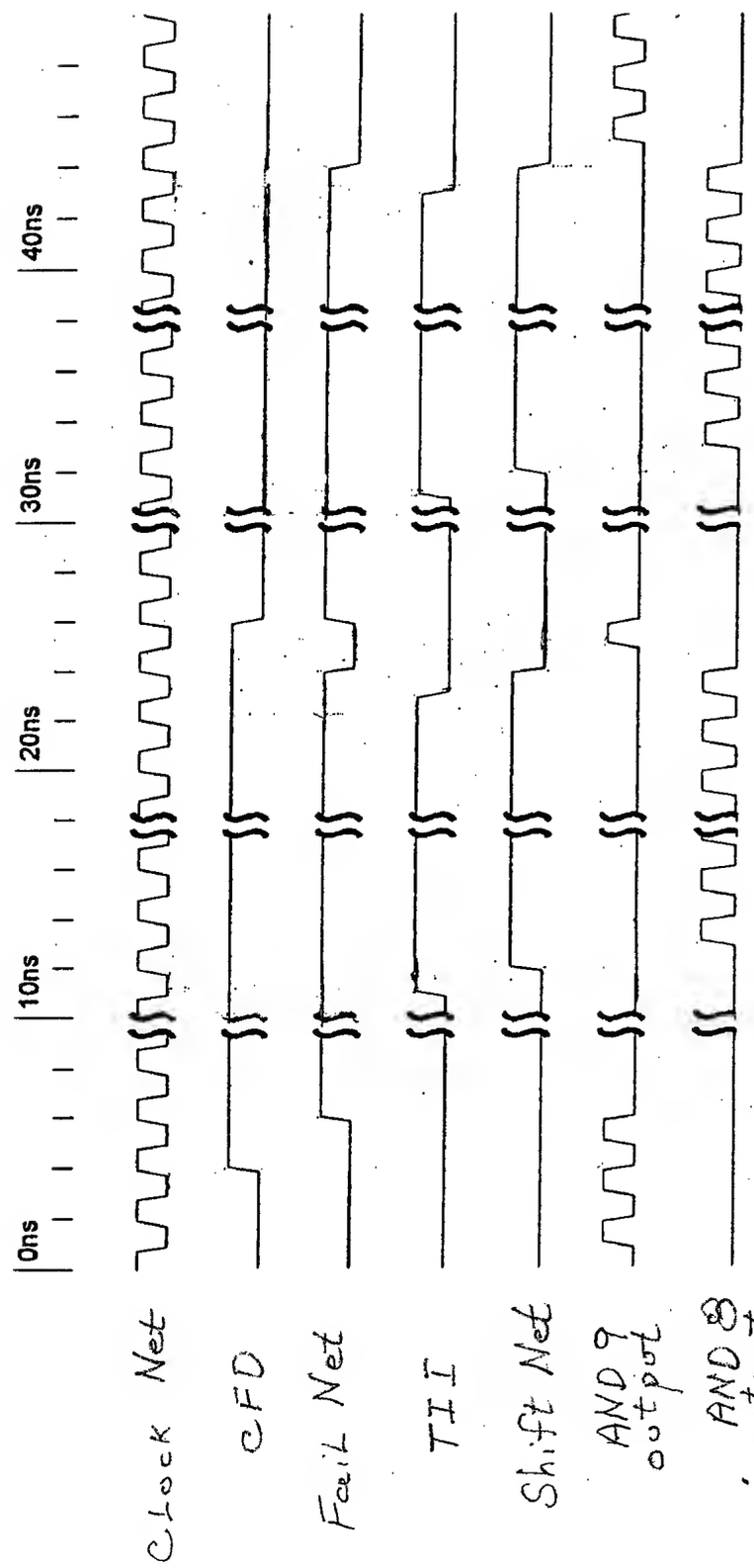
0ns
10ns
20ns
30ns
40ns
Clock Net
CFD
Fail Net
TII
Shift Net
AND 9 output
AND 8 output

Fig. 8